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Subject: Request for Certification of correction  
 PATENT NO US 7,071,069 B2  
 ISSUED July 4, 2006  
 Serial No. 10/743,247  
 Attorney Docket: CS03-046

Page 1

File: cs2003-046-request-for-certificate-of-correction.doc

To: Commissioner of Patents P.O. Box 1450 Alexandria, VA 22313-1450	
From: William J. Stoffel Reg no. 39,390 Customer no. 30,402	1735 Market St - Ste A455 Philadelphia, PA 19103-7502 USA  Work 215-670-2455 Fax 267-200-0730

Subject:	Request for Certification of correction
PATENT NO	US 7,071,069 B2
ISSUED	July 4, 2006
Serial No.	10/743,247
Docket	CS03-046
File date:	12/22/2003
Inventor:	Tan et al.
Title :	<b>Shallow Amorphizing Implant For Gettering Of Deep Secondary End Of Range Defects</b>

**Certificate  
of Correction**  
 AUG 03 2006

5

**REQUEST FOR CERTIFICATION OF CORRECTION**

Dear Sir:

Applicant requests a certificate of correction for the above mentioned patent.

<b>CERTIFICATE OF MAILING OR FACSIMILE TRANSMISSION</b>	
I hereby certify that this correspondence is being :	
<input type="checkbox"/> FAXED to the central facsimile number of patent and trademark office at the following number <b>(571) 273-8300</b> or <input checked="" type="checkbox"/> deposited with the United States Postal Service as first class mail in an envelope addressed to: Attn: Certificate of Correction branch, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450; on the date below.	
/William J. Stoffel REG # 39,390/ William J. Stoffel date July 29, 2006 Customer No. 30402	

AUG 04 2006

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Dear Madam and Sir:

- **The above patent contains signification errors as indicated on the attached certificate of correction form (SB44) (submitted in duplicate). There errors arose at the respective places in the application file as indicated below.**
- **Such errors arose through the fault of the Patent and Trademark Office, therefore patentee requests that the Certificate be issued at no cost.**
- Please note several errors appear to have been made printing the claims from the Applicant's reply to office action date Aug 04, 2005. This Office action had to be faxed to the PTO two times because of a faxing error. The second fax transmitted all pages. It appears that both faxes were entered into pairs. Possibly, some of the printing errors were made by using the 1<sup>st</sup> incomplete fax.
- Attached in the appendix are copies of pages 6 thru 9 of Applicant's reply to office action date Aug 04, 2005.

Claim 11

- **Specifically**, in issued Claim 11, col. 9, line 36, step (d), please change "SDF ," to --SDE--. For support see the Applicant's reply to office action date Aug 04, 2005, page 5, (claim 8) line 13; that shows --SDE--. Also see the originally file application, page 23, L 15. This appears to have been erroneously printed by the patent office.

Claim 20

- **Specifically**, in issued claim 20, col. 10, Line 15, please delete "or". For support see the Applicant's reply to office action date Aug 04, 2005, page 6, line 25; that shows "or" with a cross out. This appears to have been erroneously printed by the patent office.
- **Specifically**, in issued claim 20, after line 48; at the end of the claims, several lines of the claim are not printed.

AUG 04 2006

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Issued Claim 20, starting at line 43 to the end of the claim (steps (g) and g(1)) should be read as follows (showing text to be added underlined)

- (g) performing an anneal procedure comprised of a first soak step and a second spike step to recrystallize the amorphous shallow implant region and said amorphous pocket region; whereby said shallow amorphous implant region reduces the defects from the pocket implantation;
- (1) the anneal procedure comprises (1) a soak step at a temperature between 600 and 800 °C for a time between 10 and 30 seconds and (2) a spike step where the temperature ramps up to a peak temperature between 1000 and 1100 °C and a ramp down from said peak temperature to a temperature below 800 °C; said ramp up and ramp down have a rate between 200 and 300 degree° C per minute.

Therefore, please replace the entire Issued Claim 20, starting at line 15 to 48 with the following:

20. A method for a pocket implant comprising:

- a) providing a gate structure on a semiconductor substrate comprised with a first conductivity type dopant;
  - b) performing a pocket amorphizing implantation procedure to implant ions of a first conductivity type to form a pocket implant region adjacent to said gate structure, an amorphous pocket region and pocket interstitials under the amorphous pocket region;
  - c) performing a shallow amorphizing implant to form an amorphous shallow implant region and shallow implant interstitials; the amorphous shallow implant region being formed at a second depth above said amorphous pocket region; the substrate above the amorphous shallow implant region remains crystalline;
- (1) said amorphous shallow implant region is formed at a minimum depth of about 8 nm and a maximum depth of 20 nm below the substrate surface; said amorphous shallow implant region has a thickness between 5 and 10 nm;

- 
- d) performing a SDE implant to form SDE regions of a second conductivity type, in an area of said semiconductor substrate not covered by said gate structure, with said SDE regions located in a top portion of said pocket region;
  - e) forming spacers on the sidewalls of the gate structure;
  - f) performing a S/D implant procedure to form Deep S/D regions;
  - g) performing an anneal procedure comprised of a first soak step and a second spike step to recrystallize the amorphous shallow implant region and said amorphous pocket region; whereby said shallow amorphous implant region reduces the defects from the pocket implantation;
- (1) the anneal procedure comprises (1) a soak step at a temperature between 600 and 800 °C for a time between 10 and 30 seconds and  
(2) a spike step where the temperature ramps up to a peak temperature between 1000 and 1100 °C and a ramp down from said peak temperature to a temperature below 800 °C; said ramp up and ramp down have a rate between 200 and 300 degree° C per minute.

For support see the Applicant's reply to office action date Aug 04, 2005, page 6, L 25, to page 8, line 6. Also, see the originally filed application, page 26, L 12 to page 27, L 2. This appears to have been erroneously printed by the patent office.

### CONCLUSION

In conclusion, issuance of the certificate of correction is respectfully requested.

It is requested that the Examiner telephone the undersigned attorney at (215) 670-2455 should there be anyway that we could help to place this Application in condition for Allowance.

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**Charge to Deposit Account**

The Commissioner is hereby authorized to apply any fees or credits in this case, which are not already covered by check or credit card, to Deposit Account No. 502018 referencing this attorney docket. The Commissioner is also authorized to charge any additional fee under 37 CFR §1.16 and 1.17 to this Deposit Account.

Respectfully submitted,

/William J. Stoffel REG # 39,390/

William J. Stoffel

Customer No. 30402

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### Appendix

- Copy of pages 6 thru 9 of Applicant's reply to office action date Aug 04, 2005.
- **certificate of correction form (SB44) (submitted in duplicate)**

- 1 11. (ORIGINAL) The method of claim 8 wherein the pocket amorphizing implantation  
2 comprises implanting Sb or In species at an energy between 115 and 150 keV using a  
3 quad implant at a 45 degree angle to form a pocket implant to a depth between 40 and  
4 100 nm.
- 5 12.(CURRENTLY AMENDED) The method of claim 8 wherein the shallow  
6 amorphizing implant comprises: implanting As, Si, or Ge ~~or N~~ species at a dose  
7 between  $5 \times 10^{13} \text{cm}^{-2}$  and  $7 \times 10^{14} \text{cm}^{-2}$  and at an energy between 5 and 10 keV, and  
8 preferably at a 7 degree and a quad twist.
- 9 13. (ORIGINAL) The method of claim 8 wherein said amorphous shallow implant  
10 region is formed at a minimum depth of about 8 nm and a maximum depth of 20 nm  
11 below the substrate surface; said amorphous shallow implant region has a thickness  
12 between 5 and 10 nm.
- 13 14. (ORIGINAL) The method of claim 8 wherein said amorphous shallow implant region  
14 has a thickness between 5 and 10 nm.
- 15 15.(ORIGINAL) The method of claim 8 wherein the S/D implant procedure comprises:  
16 implanting As ions at a dose of between  $5 \times 10^{13}$  and  $7 \times 10^{14}$  atoms/sq-cm; an energy  
17 between 5 and 10 keV and a maximum depth between 30 and 50 nm.
- 18 16. (ORIGINAL) The method of claim 8 wherein the anneal procedure comprises: (1)  
19 a soak step at a temperature between 600 and 800 °C for a time between 10 and 30  
20 seconds and (2) a spike step where the temperature ramps up to a peak temperature  
21 between 1000 and 1100 °C and a ramp down from said peak temperature to a  
22 temperature below 800 °C; said ramp up and ramp down have a rate between 200 and  
23 300 degree °C per minute.
- 24
- 25 17. (Currently Amended ) A method of for a pocket implant comprising:  
26 a) providing a gate structure on a semiconductor substrate comprised with a first  
27 conductivity type dopant;

- 1           b) performing a pocket amorphizing implantation procedure to implant ions of a  
2                     first conductivity type to form a pocket implant region adjacent to said  
3           gate structure, an amorphous pocket region and pocket interstitials  
4           under the amorphous pocket region;
- 5           c) performing a shallow amorphizing implant to form an amorphous shallow  
6           implant region and shallow implant interstitials; the amorphous  
7           shallow implant region being formed at a second depth above said  
8           amorphous pocket region;  
9                     the substrate above the amorphous shallow implant  
10           region remains crystalline;
- 11                     (1) said amorphous shallow implant region is formed at a minimum  
12                     depth of about 8 nm and a maximum depth of 20 nm below the  
13                     substrate surface; said amorphous shallow implant region has a  
14                     thickness between 5 and 10 nm;
- 15
- 16           d) performing a SDE implant to form SDE regions of a second conductivity type, in  
17           an area of said semiconductor substrate not covered by said gate  
18           structure, with said SDE regions located in a top portion of said pocket  
19           region;
- 20           e) forming spacers on the sidewalls of the gate structure;
- 21           f) performing a S/D implant procedure to form Deep S/D regions;
- 22           g) performing an anneal procedure comprised of a first soak step and a second spike  
23           step to recrystallize the amorphous shallow implant region and said  
24           amorphous pocket region; whereby said shallow amorphous implant  
25           region reduces the defects from the pocket implantation;



- 1 (1) the anneal procedure comprises (1) a soak step at a temperature  
2 between 600 and 800 °C for a time between 10 and 30 seconds and  
3 (2) a spike step where the temperature ramps up to a peak  
4 temperature between 1000 and 1100 °C and a ramp down from said  
5 peak temperature to a temperature below 800 °C; said ramp up and  
6 ramp down have a rate between 200 and 300 degree° C per minute.  
7
- 8 18. (ORIGINAL) The method of claim 17 wherein the pocket amorphizing implantation  
9 comprises implanting Sb or In species at an Energy between 115-150 keV using a  
10 quad implant at a 45 degree angle to form a pocket implant region to a depth between  
11 40 and 100 nm.
19. (ORIGINAL) The method of claim 17 wherein said amorphous pocket region is formed at a  
depth range between 40 and 100 nm; said amorphous pocket region has a thickness between  
10 and 20 nm; the substrate above the amorphous pocket region remains crystalline.
20. (Currently Amended) The method of claim 17 wherein the shallow amorphizing implant  
comprises: implanting As, Si, or Ge species at a dose greater than  $5 \times 10^{13} \text{cm}^{-2}$  and at an  
energy between 5 and 10 keV, and ~~preferably~~ at a 7 degree and a quad twist.
21. (New ) The method of claim 1 wherein said amorphous shallow implant region is not a halo  
region.
22. (NEW) The method of claim 1 wherein said wherein the shallow amorphizing implant  
comprises: implanting As, Si, or Ge species; said first conductivity type is p-type and said  
second conductivity type is n-type.
23. (NEW) The method of claim 1 wherein said wherein the shallow amorphizing implant  
comprises: implanting Si , or Ge species.

S/N 10/743,247

Inventor: Tan et al.

Reply to the Office action dated August 04, 2005

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24. (NEW) The method of claim 17 wherein said wherein the shallow amorphizing implant comprises: implanting Si, Ge or As species.

## UNITED STATES PATENT AND TRADEMARK OFFICE CERTIFICATE OF CORRECTION

Page 1 of 2

PATENT NO. : US 7,071,069  
APPLICATION NO.: 10/743,247  
ISSUE DATE : July 4, 2006  
INVENTOR(S) : Chong Foong Tan et al.

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

- \* In issued Claim 11, col. 9, line 36, step (d), "SDF," changed to --SDE--.
- \* Please replace the entire Issued Claim 20, starting at col 10, lines 15 to 48 with the following:

20. A method for a pocket implant comprising:

- a) providing a gate structure on a semiconductor substrate comprised with a first conductivity type dopant;
- b) performing a pocket amorphizing implantation procedure to implant ions of a first conductivity type to form a pocket implant region adjacent to said gate structure, an amorphous pocket region and pocket interstitials under the amorphous pocket region;
- c) performing a shallow amorphizing implant to form an amorphous shallow implant region and shallow implant interstitials; the amorphous shallow implant region being formed at a second depth above said amorphous pocket region;  
the substrate above the amorphous shallow implant region remains crystalline;  
(1) said amorphous shallow implant region is formed at a minimum depth of about 8 nm and a maximum depth of 20 nm below the substrate surface; said amorphous shallow implant region has a thickness between 5 and 10 nm;
- d) performing a SDE implant to form SDE regions of a second conductivity type, in an area of said semiconductor substrate not covered by said gate structure, with said SDE regions located in a top portion of said pocket region;
- e) forming spacers on the sidewalls of the gate structure;
- f) performing a S/D implant procedure to form Deep S/D regions;

MAILING ADDRESS OF SENDER (Please do not use customer number below):

William Stoffel  
1735 Market St - Ste A455  
Philadelphia, PA 19103-7502 USA

This collection of information is required by 37 CFR 1.322, 1.323, and 1.324. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1.0 hour to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Attention Certificate of Corrections Branch, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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AUG 04 2006

**UNITED STATES PATENT AND TRADEMARK OFFICE  
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(claim 20 continued)

g) performing an anneal procedure comprised of a first soak step and a second spike step to recrystallize the amorphous shallow implant region and said amorphous pocket region; whereby said shallow amorphous implant region reduces the defects from the pocket implantation;

(1) the anneal procedure comprises (1) a soak step at a temperature between 600 and 800 °C for a time between 10 and 30 seconds and (2) a spike step where the temperature ramps up to a peak temperature between 1000 and 1100 °C and a ramp down from said peak temperature to a temperature below 800 °C; said ramp up and ramp down have a rate between 200 and 300 degree° C per minute.

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